REMARKS

Claims 1-11 have been examined on their merits.

Applicant herein cancels claim 4 without prejudice and/or disclaimer.

Applicant herein amends claims 1 and 5 to recite that the parameter generation is performed at a first frequency and the retrieval of the generated parameters is done at a second frequency, wherein the second frequency is slower than the first frequency.

Claims 1-3 and 5-11 are all the claims presently pending in the application.

1.   Claims 1-4 stand rejected under 35 U.S.C. § 112 (2nd para.) as allegedly mixing statutory classes. The rejection of claim 4 is now moot due to its cancellation.

Applicant herein amends claim 1 to remove the alleged nested apparatus claim from the preamble of claim 1. Applicant submits that the § 112 (2nd para.) rejection of claims 1-3 has been overcome, and respectfully requests withdrawal of same.

2.   Claims 1-7 and 9-11 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Nakano *et al.* (U.S. Patent No. 4,777,618). Applicant traverses the rejection of claims 1-7 and 9-11 for at least the reasons discussed below.

To support a conclusion that a claimed invention lacks novelty under 35 U.S.C. § 102, a single source must teach all of the elements of a claim. *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1379 (Fed. Cir. 1986). A claim is anticipated only if each and every element as set forth in the claim is found either expressly or inherently in a single prior art

reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

A single source must disclose all of the claimed elements arranged as in the claim. *Richardson*

v. Suzuki Motor Co., 868 F.2d 1226, 1236 (Fed. Cir. 1989). Rejections under 35 U.S.C. § 102

are proper only when the claimed subject matter is identically disclosed or described in the prior

art. Thus, the cited reference must clearly and unequivocally disclose every element and

limitation of the claimed invention.

With respect to claim 1, Nakano *et al.* fails to teach or suggest at least the processing of

output signals generated from an electronic device under test at a first frequency in response to

simulated input signals and the retrieval of the stored processing results at a second frequency,

where the second frequency is slower than the first frequency. Nakano *et al.* discloses an engine

control simulator 20 for analyzing the operating conditions of the ECU 14 for controlling an

engine 12 mounted onto a motor vehicle 10 where:

> [I]n storing the internal information of the computer [i.e., computer of ECU
> 14], which is stored in the random access memory, the register and the like
> together with the input and output signals of the computer and indicating the
> same, the internal information of the computer, which is added thereto with
> the time information, at which the internal information is read out, is stored,
> and the input and output signals of the computer are synchronized with the
> time information to indicate the internal information, so that the changes of
> the internal information corresponding to the changes of the input and output
> signals, can be indicated in synchronism with each other. In consequence, the
> operating conditions of the computer can be properly analyzed. (col. 6, lines
> 10-24; *see also,* col. 8, line 31 through col. 13, line 57).

Contrary to the Patent Office's analysis, nowhere do Nakano *et al.* teach or suggest generating, at

a first frequency, parameters based on simulated input signals and accessing those stored

parameters at a second frequency, which is slower than the first frequency. In fact, Nakano *et al.*

has nothing to do with access frequency, let alone access frequency of stored parameters corresponding to signals output by units under test, as recited independent claim 1. Instead, Nakano *et al.* provide a method where "input and output signals of the computer [under test] are synchronized with the time information to indicate the internal information [of the computer under test], so that the changes of the internal information corresponding to the changes of the input and output signals, can be indicated in synchronism with each other" (*see* col. 6, lines 17-22 of Nakano *et al.*). In sum, Nakano *et al.* fail to teach or suggest a method wherein output signals, based on input stimuli, are generated and stored at a greater rate than they are accessed.

Based on the foregoing reasons, Applicant submits that Nakano *et al.* fail to teach or suggest all of the claimed elements as arranged in claim 1. Therefore, under *Hybritech* and *Richardson*, Nakano *et al.* clearly cannot anticipate the present invention as recited in independent claim 1. Thus, Applicant submits that claim 1 allowable, and further submits that claims 2 and 3 are allowable as well, at least by virtue of their dependency from claim 1. Applicant respectfully requests that the Patent Office withdraw the § 102(b) rejection of claims 1-3.

With respect to independent claim 5, Applicant submits that claim 5 is allowable for at least reasons analogous to those discussed above with respect to claim 1, in that Nakano *et al.* fail to teach or suggest a circuit that processes of output signals generated from an electronic device under test at a first frequency in response to simulated input signals and a microprocessor that retrieves the stored processing results at a second frequency, where the second frequency is slower than the first frequency. Therefore, under *Hybritech* and *Richardson*, Applicant submits

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that claim 5 is allowable, and further submits that claims 6-11 are allowable as well, at least by virtue of their dependency from claim 5. Applicant respectfully requests that the Patent Office withdraw the § 102(b) rejection of claims 5-11.

3.   Claim 8 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Nakano *et al.* in view of Hanselmann, *Hardware-in-the-Loop Simulation Testing and Integration into a CADSD Toolset*, IEEE International Symposium on Computer-Aided Control System Design 1998. Applicant traverses the rejection of claim 8 for at least the reasons discussed below.

Hanselmann discloses, *inter alia*, a simulator that outputs various stimuli to a unit under test. *See, e.g.,* Figure 2 of Hanselmann. However, Hanselmann fails to teach or suggest at least the circuit generating parameters, at a first frequency, and a microprocessor that accessed the stored parameters at a second frequency that is slower than the first frequency. Since claim 8 depends upon claim 5 and since Hanselmann does not cure the deficient teachings of Nakano *et al.* with respect to claim 5, Applicant submits that claim 8 is patentable at least by virtue of its dependency from claim 5. Therefore, Applicant respectfully requests that the rejection of claim 8 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

AMENDMENT UNDER 37 C.F.R. § 1.116
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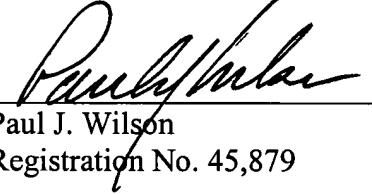
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